



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,150	08/02/2001	Jin Chuan Bai	MM4460	7226
1109	7590	12/27/2004	EXAMINER	
ANDERSON, KILL & OLICK, P.C. 1251 AVENUE OF THE AMERICAS NEW YORK,, NY 10020-1182			ZARNEKE, DAVID A	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/921,150

Applicant(s)

BAI, JIN CHUAN

Examiner

David A. Zarneke

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/6/04 with respect to the rejections of claims over Applicant's admitted prior art have been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Cook et al., US Patent 6,331,446 and Lau, Flip Chip Technologies, McGraw-Hill, 1996, p 534 & 535. The rejection will be detailed below.

With respect to claim 7, Applicant's arguments stating that Cook's underfill (26) isn't an encapsulant as required by the claim because the term underfill is defined as a material that fills a gap between two layers, which therefore means that (26) is clearly different from the claimed encapsulant.

The examiner asserts that if the definition supplied by applicant is the only definition of the term underfill, what/how does Cook's underfill (26) actually underfill? Obviously, it doesn't "underfill" anything. Therefore, either the term was miss used in Cook or the term underfill has a broader accepted meaning than the literal one supplied by applicant. Either way, you can call it what you want, it performs the same function as in the claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Lau, Flip Chip Technologies, McGraw-Hill, 1996, p 534 & 535, and Cook et al., US Patent 6,331,446, and Takeuchi et al., US Patent Application Publication 2001/0039891.

Booth teaches a direct chip attachment process comprising:

- 1) preparing a substrate (1) having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface with the first surface having a first plurality of bond pads (8) electrically connected to the substrate;
- 2) screen printing [mask screening] (3, 20+) a plurality of conductive elements (4) on the chip-mounting area of the substrate in direct alignment over each of said first

plurality of bond pads (Figure 6), wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant (2) by a mask screening (3, 20-21), which is a type of printing process, on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant formed by printing is adapted to have a top surface thereof formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant (Figure 9); and

4) preparing at least one semiconductor chip (6) having a second plurality of bond pads (Figure 14) formed on a surface thereof and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the second bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface (Figures 5-9 & 14).

Booth, which teaches the bond pads as being formed on the substrate, fails to teach the bond pads of the substrate as being formed in the substrate.

Lau teaches that it is well known in the art to form the bond pads in the substrate (figure 1A).

The forming of bond pads ON a substrate or IN a substrate are both more than well-known in the art equivalent bond pad structures, as taught by Lau Figures 17.13, 17.14 and 17.15.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); *In re Mostovych* 144 USPQ 38 (CCPA 1964); *In re Leshin* 125 USPQ 416 (CCPA 1960); *Graver Tank & Manufacturing Co. V. Linde Air Products Co.* 85 USPQ 328 (USSC 1950).

Booth also fails to teach the steps 5 and 6, namely the encapsulating of the chip and the implanting of solder balls onto the opposite side of the substrate.

Cook teaches that it is well known in the art to encapsulate a chip and to implant solder balls to the opposite side of the substrate (Figure 3).

It would have been obvious to one of ordinary skill in the art to use the chip encapsulation and solder ball implantation of Cook in the invention of Booth because these are conventional steps used in the packaging of a chip.

The use of conventional materials to perform their known functions in a conventional process is obvious. *In re Raner* 134 USPQ 343 (CCPA 1962).

Takeuchi is cited as support for the assertion that mask screening is the same as screen printing. The abstract teaches that a screen mask is used for screen printing. Further, the specification is replete with instances of talking about a mask or screen mask used in screen printing.

Regarding claim 2, Booth teaches the conductive elements as being conductive bumps (3, 1).

With respect to claim 3, while Booth teaches a conductive adhesive as the conductive element (3, 21+), tin, lead, or a tin/lead alloy conductive element is an equivalent type of conductive element that is commonly used in the art.

While Booth lists a few undesirable attributes of solder alloys, Booth states that solder alloys are pervasively used to interconnect components to carriers (1, 22+).

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 5, Booth teaches the use of conductive metal contacts (8), aka bond pads, electrically connected to chip sites on the surface of the substrate (2, 52+).

Regarding claim 6, Booth teaches the 2nd surface of the chip as having no bond pads (Figure 14).

With respect to claim 7, Booth fails to teach the 2nd encapsulant as exposing the outside surface of the chip, which has no bond pads.

Cook teaches a process of underfilling a C4 IC package comprising a 2nd encapsulant that forms a fillet around the edges of the chip without encapsulating the outer surface of the chip (Figure 3).

It would have been obvious to one of ordinary skill in the art to use the fillet of Cook in the invention of Booth because Cook teaches that the fillet seals the edges of

the chip and the underfill such that moisture migration is inhibited and chip and/or underfill cracking is prevented (2, 56+).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Lau, Flip Chip Technologies, McGraw-Hill, 1996, p 534 & 535, and Cook et al., US Patent 6,331,446, and Takeuchi et al., US Patent Application Publication 2001/0039891, as applied to claim 1 above, and further in view of Lai, US Patent 6,323,066.

Booth, Cook, Lau and Takeuchi all fail to teach the use of a heat sink that is encapsulated by the 2nd encapsulant.

Lai teaches a heat-dissipating structure comprising attaching a chip to a substrate, attaching a heat sink to the substrate and over the chip, and then encapsulating the heat sink and the chip (Figure 6).

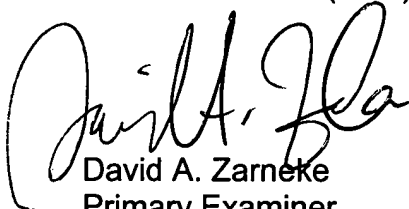
It would have been obvious to one of ordinary skill in the art to use the heat sink of Lai in the combined invention of Booth, Cook, Lau and Takeuchi because Lai teaches that this type of heat sink arrangement prevents resin flow during the molding process and also prevents the heat sink from causing a thermal compressive stress in the chip during cooling (2, 30+).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571)-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David A. Zarneke
Primary Examiner
December 21, 2004